Supplementary Information for:

A Ferroelectric Semiconductor Field-Effect Transistor

Mengwei Si[1,4], Atanu K. Saha[1], Shengjie Gao[2,4], Gang Qiu[1,4], Jingkai Qin[1,4], Yuqin Duan[1,4], Jie Jian[3], Chang Niu[1,4], Haiyan Wang[3], Wenzhuo Wu[2,4], Sumeet K. Gupta[1], and Peide D. Ye[1,4,*]

[1]*School of Electrical and Computer Engineering, Purdue University, West Lafayette, Indiana 47907, United States*

[2]*School of Industrial Engineering, Purdue University, West Lafayette, Indiana 47907, United States*

[3]*School of Materials Science and Engineering, Purdue University, West Lafayette, In 47907, United States*

[4]*Birck Nanotechnology Center, Purdue University, West Lafayette, Indiana 47907, United States*

*Address correspondence to: yep@purdue.edu (P.D.Y.)

1. Piezoelectric coefficient and DART-PFM data

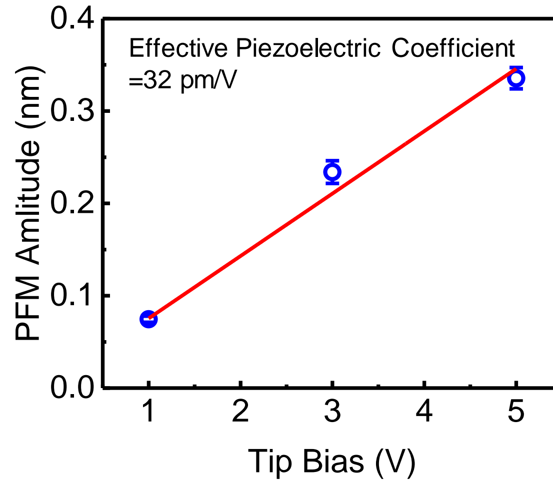

Figure S1. Effective piezoelectric coefficient of a 78.7 nm thick α-In_2Se_3 flake, measured by PFM.

To extract the piezoelectric coefficient, different AC voltages are applied on the sample from the conductive AFM tip which shows a linear relationship between the mechanical deformation (PFM amplitude) and the electric field, as shown in Fig. S1. The piezoelectric coefficient (d_{33}) of the α-In_2Se_3 flake is 32 pm/V. It should be noticed that the d_{33} obtained here is effective piezoelectric coefficient ($d_{33,eff}$), which is affected by other tensor elements from the sample and tip-sample electrostatic interaction.

Fig. S2 shows the raw data of single point DART-PFM hysteresis loop measurement measured at room temperature. Fig. S2a shows the applied voltage biases versus time. Two cycles of triangular voltage waves are applied with both on field and off field PFM measurements, as shown in Fig. S2b. Fig. S2c-e show the PFM amplitude, phase1 and phase2 signals, measured using MSM structure. Fig. S2f-h show the PFM amplitude, phase1 and phase2 signals, measured using MOS structure. A clear ferroelectric polarization switching can be seen on both phase1 and

phase2 signals, at both on field and off field and for both MSM and MOS structure. The raw data itself confirms the ferroelectricity and switchable polarization of α-In_2Se_3 for FeS-FET application.

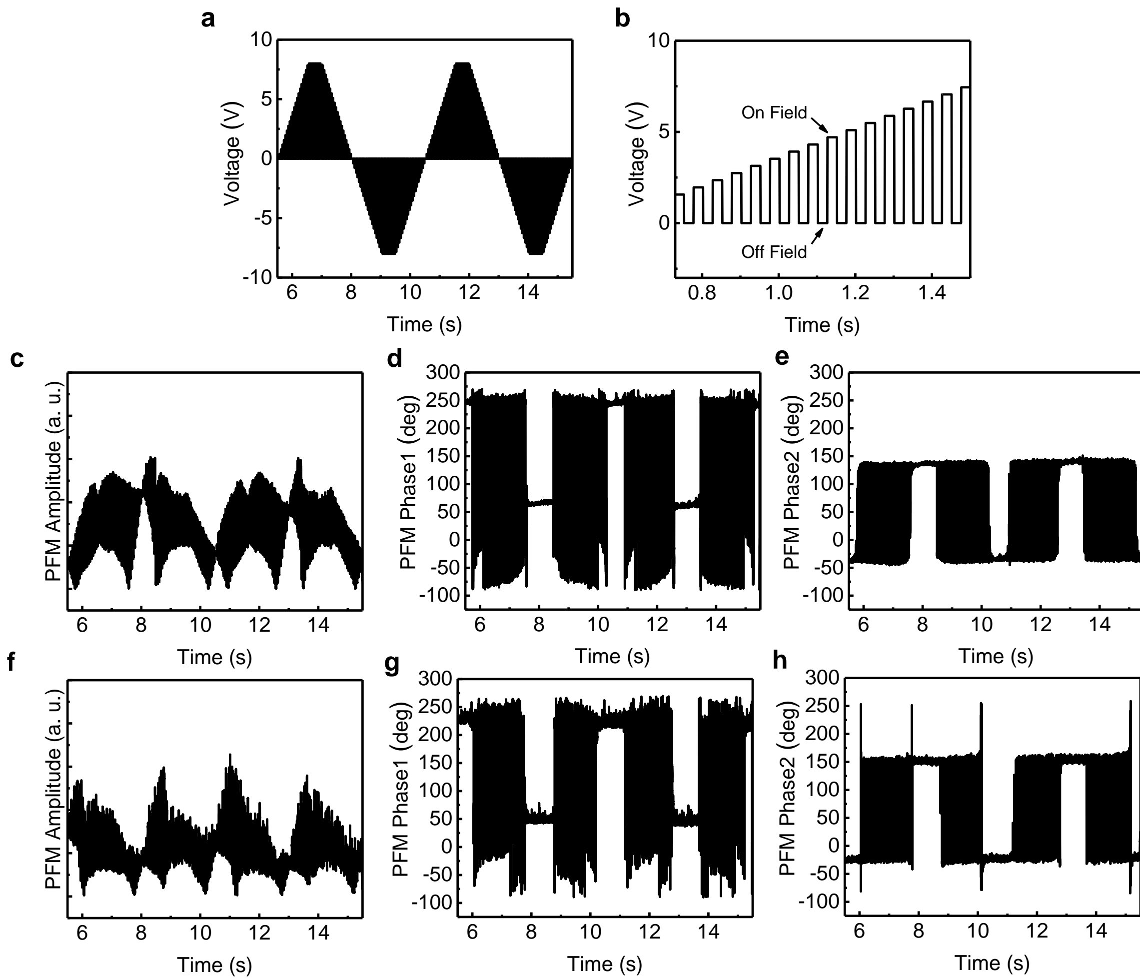

Figure S2. Raw data of single point DART-PFM hysteresis loop measurements at room temperature. **a,** Bias versus time and **b,** zoom-in plot of **a**, showing on field and off field measurements. **c,** Amplitude, **d,** phase1, and **e,** phase2 results in MSM structure. **f,** Amplitude, **g,** phase1, and **h,** phase2 results in MOS structure.

2. Unpassivated α-In_2Se_3 FeS-FETs

Fig. S3 shows the I_D-V_{GS} characteristics of a representative α-In_2Se_3 FeS-FET without ALD passivation, measured by double gate voltage sweep and at different V_{DS}. The device has a channel length (L_{ch}) of 1 μm, channel thickness (T_{ch}) of 62.2 nm. The transfer curve shows clear clockwise hysteresis loop and a large memory window over 70 V. A high on/off ratio over 10^7 at V_{DS}=0.5 V between on- and off-states is also achieved. Fig. S4 investigates the impact of gate voltage sweep range and sweep time on the performance of α-In_2Se_3 FeS-FETs and are measured on a α-In_2Se_3 FeS-FET with L_{ch}=1 μm and T_{ch}=78 nm. Fig. S4a and Fig. S4b show the I_D-V_{GS} characteristics measured at different V_{GS} sweep ranges and different sweep time (sweep time controlled by the number of V_{GS} step, the fastest measurement time of the whole loop is about 1 s). Fig. S4c and Fig. S4d plot the remnant I_D and coercive V_{GS} versus gate voltage sweep range. The gate voltage sweep range dependence suggests more polarization charge is generated by higher gate voltage. Fig. S4e and Fig. S4f show the remnant I_D and coercive V_{GS} versus sweep time. The I_D-V_{GS} curve has a weak sweep speed dependence, indicating the mobile trapped charges play a minor role in device characteristics.

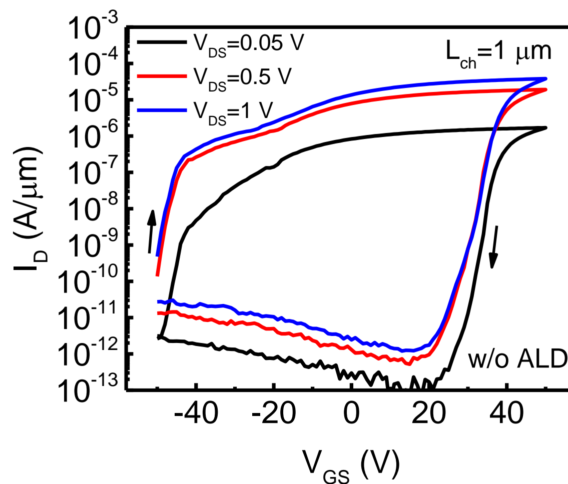

Figure S3. I_D-V_{GS} characteristics of an α-In_2Se_3 FeS-FET without ALD passivation, measured at V_{DS}=0.05 V and different V_{GS} sweep ranges. The device has a channel length (L_{ch}) of 1 μm, channel thickness (T_{ch}) of 62.2 nm.

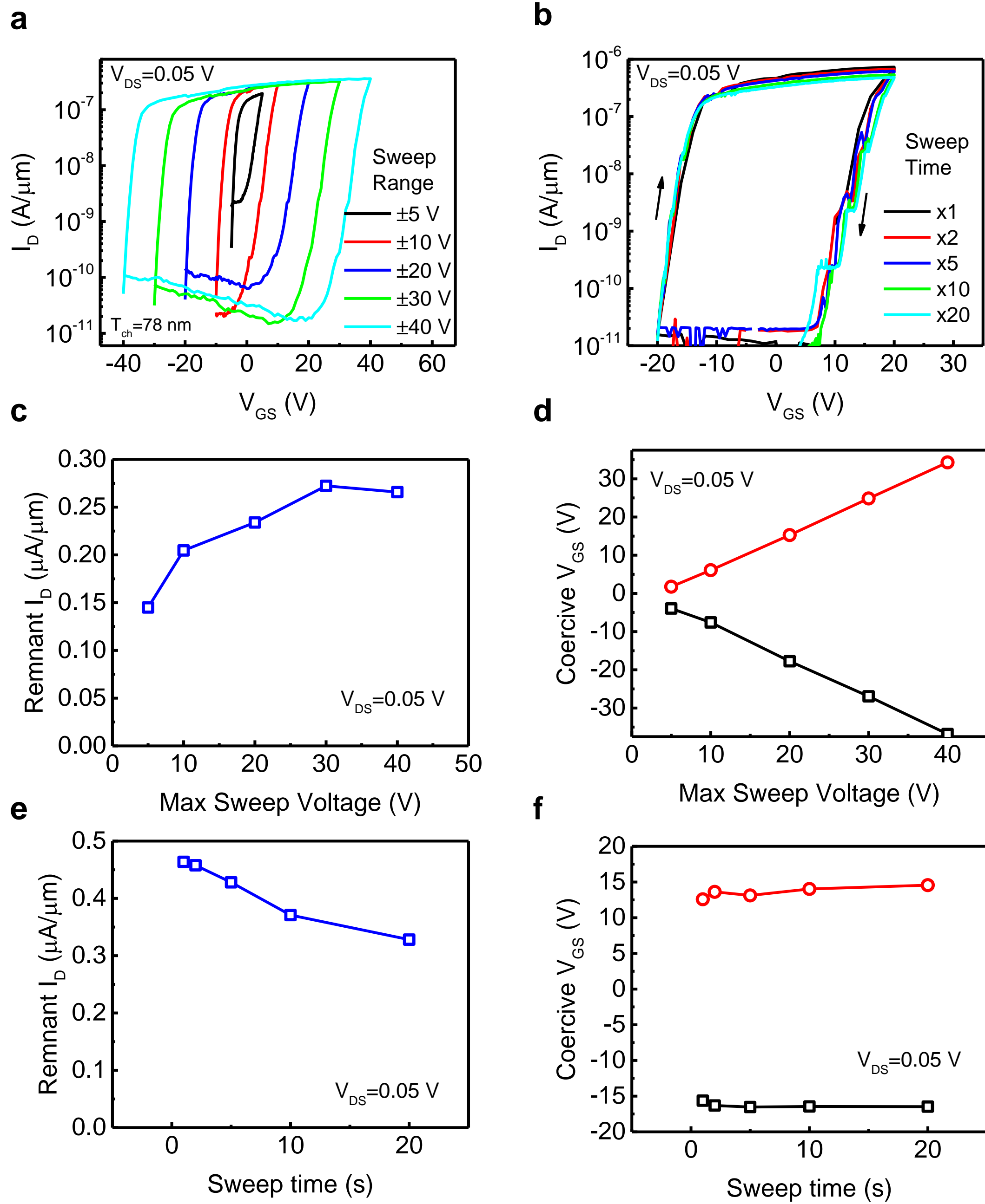

Figure S4. **a,** I_D-V_{GS} characteristics of an α-In_2Se_3 FeS-FET without ALD passivation, measured at V_{DS}=0.05 V and different V_{GS} sweep ranges. **b,** I_D-V_{GS} characteristics of the same α-In_2Se_3 FeS-FET, measured at V_{DS}=0.05 V and different sweep times. **c,** Remnant I_D measured at different V_{GS} sweep ranges on the same device. **d,** Coercive V_{GS} (V_{GS} at I_D= 10 nA/μm) measured at different V_{GS} sweep ranges on the same device. **e,** Remnant I_D measured at different V_{GS} sweep times on the same device. **f,** Coercive V_{GS} (V_{GS} at I_D= 10 nA/μm) measured at different V_{GS} sweep times on the same device.

3. Low temperature and Hall measurements

In the α-In_2Se_3 FeS-FETs with 90 nm SiO_2 as gate insulator, the hysteresis loop is clockwise. The hysteresis direction is same as the hysteresis direction induced by charge trapping. To distinguish from charge trapping induced hysteresis loop and prove the ferroelectricity, low temperature I-V and Hall measurement are performed at 80 mK. The clockwise hysteresis still exists at very low temperature measurement down to 80 mK and the hysteresis window is very similar to the room temperature results, as shown in Fig. S5a and S5b. It is well-known that charge trapping process is related with thermal activation and has strong temperature dependence. The threshold voltage shift and transistor hysteresis are reduced significantly at low temperature [1,2]. Therefore, the existence of similar hysteresis window at low temperature of 80 mK supports the existence of ferroelectricity and ferroelectric polarization switching as the origin of the hysteresis.

Fig. S5c and S5d show Hall measurements of R_{xx} and R_{xy} versus magnetic field (B) measured at V_{GS}=20 V (same device as Fig. S5a). The corresponding carrier density (n_{2D}) and Hall mobility (μ_H) are determined to be $n_{2D}=1.32\times10^{13}$ cm^{-2} and μ_H=223.4 cm^2 V^{-1} s^{-1}. Fig. S5e and S5f show some additional Hall measurement data measured at V_{GS}=30 V and with B field measured bi-directionally (forward and reverse), suggesting no ferromagnetic property exists in this material.

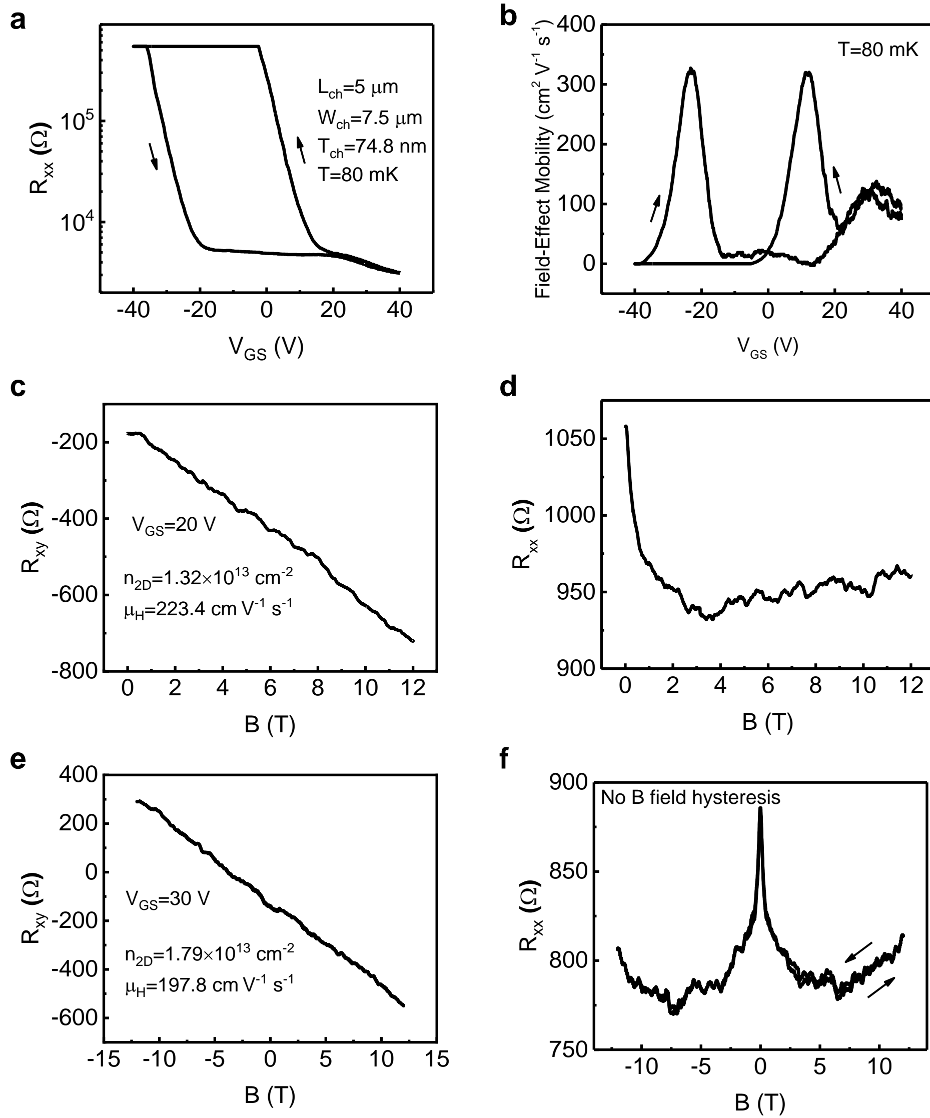

Figure S5. a, R_{xx}-V_{GS} characteristics of a α-In_2Se_3 FeS-FET with 90 nm SiO_2 as gate dielectric, 10 nm Al_2O_3 capping and using two terminal setup. The device has a channel length of 5 μm, channel width of 7.5 μm and channel thickness of 74.8 nm. All data in this figure are measured on the same device and at very low temperature of 80 mK. **b,** Field-effect mobility calculated from **a**. **c,** R_{xy} versus B field characteristics measured at V_{GS}=20 V, showing a 2D electron density of 1.32×10^{13} cm^{-2} and a hall mobility of 223.4 cm^2 V^{-1} s^{-1}. **d,** R_{xx} versus B field characteristics at V_{GS}=20 V, showing a negative magnetoresistance with quantum oscillations due to low carrier mobility. **e,** R_{xy} versus B field characteristics measured at V_{GS}=30 V, showing a 2D electron density of 1.79×10^{13} cm^{-2} and a Hall mobility of 197.8 cm^2 V^{-1} s^{-1}. **f,** R_{xx} versus B field characteristics measured bi-directionally at V_{GS}=30 V, showing a weak-localization-like negative magnetoresistance and no obvious B field hysteresis.

4. Channel thickness dependence in α-In_2Se_3 FeS-FETs

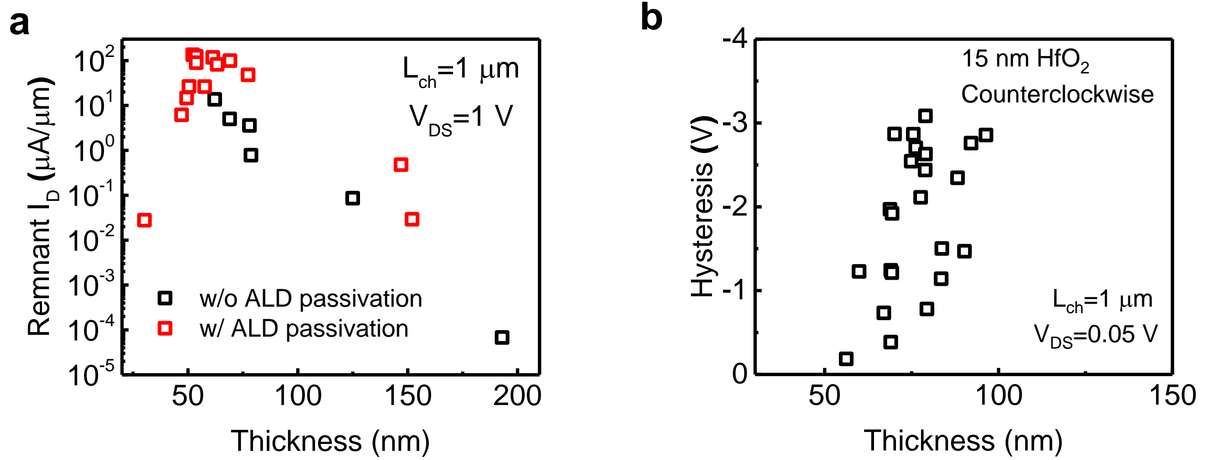

Figure S6. **a,** Channel thickness dependence and comparison of remnant drain current (at V_{GS}=0 V and V_{DS}=1 V in forward sweep) versus channel thickness of α-In_2Se_3 FeS-FETs (90 nm SiO_2) with and without ALD Al_2O_3 passivation. Significant on-current improvement is achieved by ALD Al_2O_3 passivation. **b,** Hysteresis versus thickness for α-In_2Se_3 FeS-FETs with 15 nm HfO_2 as gate insulator and with 10 nm ALD Al_2O_3 passivation.

Fig. S6a shows the channel thickness dependent remnant I_D of the α-In_2Se_3 FeS-FETs with I_D-V_{GS} curve measured at V_{DS}=1 V. Devices with and without ALD Al_2O_3 passivation are compared. The remnant I_D versus channel thickness has a peak position at around 50-70 nm, and decreases exponentially while T_{ch} increases or decreases beyond this thickness range. For thicker channel, the reason of the decrease is because the maximum voltage applied (40-50 V) is not sufficiently high to trigger the ferroelectric polarization switching. For thinner channel, this might be due to the ferroelectricity in α-In_2Se_3 is getting weaker in thinner channel, but it hasn't been clearly understood yet at current stage. Therefore, the thickness dependence also suggests the ferroelectric polarization is critical to the performance and operation of the α-In_2Se_3 FeS-FETs. The maximum remnant I_D at V_{DS}= 1V in devices with ALD passivation (135 μA/μm) is found to be significantly higher (nearly one order of magnitude) than that of devices without ALD passivation (13.7 μA/μm). The hysteresis window size is found to have a wide distribution versus

thickness, as shown in Fig. S6b. The strong correlation between channel thickness and switching voltages is not obvious. This is another evidence of the competition between the bottom surface conduction and the top surface conduction. If the surface Fermi level pinning and surface passivation of the α-In_2Se_3 Fe-FET can be further engineered and improved, the uniformity of the hysteresis window must be improved.

5. Discussions on the accuracy of field-effect mobility

The field effect mobility (μ_{FE}) is a defined as[3],

$$\mu_{FE} = \frac{Lg_m}{WC_{ox}V_{DS}} \tag{1}$$

$$g_m = \frac{dI_D}{dV_{GS}} \tag{2}$$

The transconductance (g_m) is usually extracted from the transfer (I_D-V_{GS}) characteristics of the devices. It is no doubt that the μ_{FE} can always been calculated from eqns. (1) and (2). However, the accuracy of the μ_{FE} need further discussion because μ_{FE} may not be accurate to measure the intrinsic mobility (μ) of the material. But it can reflect transport property of the material and the related device. There are two possible origins for the inaccurate estimation.

The first is because of the gate voltage dependence of intrinsic mobility[4]. The conductance is $\sigma = n_{ch}q\mu$, and channel carrier density $n_{ch} = C_{ox}(V_G - V_T)/q$. Thus, without considering the contact resistance, μ_{FE} can be re-write as,

$$\mu_{FE} = \frac{1}{C_{ox}}\frac{d\sigma}{dV_G} \tag{3}$$

$$\mu_{FE} = \mu + (V_G - V_T)\frac{d\mu}{dV_G} \tag{4}$$

From eqn. (4), μ_{FE} is under-estimated if μ become smaller at higher V_G.

The second origin is the Schottky contact resistance (R_C) (this time μ is assumed to be a constant for simplicity). So, we have the conductance and μ_{FE} re-write as,

$$\sigma = \frac{1}{R_c + \frac{1}{n_{ch}q\mu}} \tag{5}$$

$$\mu_{FE} = \frac{1}{(1+n_{ch}q\mu R_c)^2}\left(\mu - n_{ch}q\mu(V_G - V_T)\frac{dR_c}{dV_G}\right) \tag{6}$$

If R_C is a constant, μ_{FE} is under-estimated as shown in eqn. (7).

$$\mu_{FE} = \frac{\mu}{(1+n_{ch}q\mu R_c)^2} \tag{7}$$

If R_C is not a constant and becomes smaller at higher V_G, μ_{FE} can be either over- or under-estimated depends on the R_C properties.

6. Theory and simulation of FeS-FET

Device level simulations have been conducted to investigate the clockwise and counterclockwise hysteresis in the I-V characteristics of FeS-FET. More specifically, we have performed physics based self-consistent simulation of FeS-FET devices by coupling Poisson's equation, Ginzburg-Landau equation and 2D charge equation. For simplicity, a 1D cut from the source to gate region (along z-axis) of FeS-FET device has been adopted in our simulation framework. A van der Waals gap is assumed between the source/drain contacts and the semiconductor channel because of the 2D layered nature of α-In_2Se_3. Now, according to the Ginzburg-Landau theory, an equation for polarization and electric field can be written as,

$$E_{FE} + K(\nabla^2 P) = \alpha P + \beta P^3 \quad (1)$$

Here, P is the polarization, E_{FE} is the electric-field and K is the domain coupling coefficient of the ferroelectric semiconductor and all of them are defined for out-of-plane direction. Also, α and β are the effective Landau coefficients that describe the dielectric stiffness of the ferroelectric semiconductor material. The P-E relation by assumption is shown in Fig. S7. Now, the total displacement (D) in each layer can be defined as,

$$D = \epsilon_0 \epsilon_r E_{FE} + P$$

Here, ϵ_0 and ϵ_r are the vacuum and background permittivity, respectively. The Poisson's equation within the ferroelectric semiconductor layer can be written as,

$$-\epsilon_r \frac{\partial^2 \phi}{\partial z^2} = -\frac{\partial P}{\partial z} + \rho_f \quad (2)$$

$$\rho_f = q(-n + p)$$

Here, ϕ is the electrostatic potential, ρ_f is the mobile charge density. n and p are the electron density and hole density, respectively and have been calculated by using the following equations.

$$n = \frac{g_C}{t_l} \times kT \times \log\left(1 + \exp\left(\frac{E_F - E_C}{kT}\right)\right); \quad g_C = \frac{2m_C^*}{\pi\hbar^2} \quad (3)$$

$$p = \frac{g_V}{t_l} \times kT \times \log\left(1 + \exp\left(\frac{E_V - E_F}{kT}\right)\right); \quad g_V = \frac{2m_V^*}{\pi\hbar^2} \quad (4)$$

Here, g_C and g_V are the 2D density of states of electron and hole, respectively. m_C^* and m_V^* are the effective mass of electron and hole, respectively. E_C, E_V and E_F are the conduction-band energy, valence-band energy and fermi-level energy, respectively. Also, k is the Boltzmann constant, $\hbar$ is the reduced Plank's constant, t_l is the thickness of each α-In_2Se_3 layer and T is the temperature. In simulation, source electro-chemical potential has been assumed to be equal to the channel fermi-level. Finally, to get the electrostatic device characteristics we solve equation (1)-(4) self consistently to calculate polarization distribution, charge and potential profile.

From the self-consistent electrostatic simulation, we get the value of electron and hole charge density. By assuming the electron is the dominant contributor in the conduction mechanism, a drift current has been approximated by using the following equation.

$$I'_{DS} = [Q'_e + 1 \times 10^{-7} Q'_h] \times \mu \times \frac{V_{DS}}{L_{CH}}$$

$$Q_{e(h)}' = \sum_{i=1}^{n} q \times t_l n(p)_i$$

Here, I'_{DS} is the current per unit area. $Q_{e(h)}'$ is the channel electrons (holes) per unit area, respectively, which have been calculated by summing up the mobile electron (hole) charges in all the α-In_2Se_3 layers.

The coupled ferroelectric and semiconducting nature of α-In_2Se_3 is critical to analyze for understanding the device operation of FeS-FET. Each of the α-In_2Se_3 layers can exhibit either a

positive or negative polarization and that polarization can be switched by applying a gate voltage. However, the extent of polarization switching dependents on the amount of electric field in the α-In_2Se_3 channel and that further is dependent on the gate dielectric thickness for an applied gate voltage. To that effect, we consider two different EOT: high EOT (30 nm) and low EOT (0.5 nm) to analyze the device operations.

- High EOT devices:

First, let us assume that the applied gate voltage is highly negative (-35 V) and therefore, all the α-In_2Se_3 layers exhibit polarization down (as shown in Fig. S8b(i). Now, with the increase in gate voltage, polarization starts to change and the bottom α-In_2Se_3 layer (at gate oxide/semiconductor interface) conduction band goes below the fermi level (Fig. S8b(i)-(iii)). Consequentially, electron density increases near the bottom α-In_2Se_3 layer and that gives rise to an increase in channel current as shown in Fig. S8b(i)-(iii). At such scenario, bottom α-In_2Se_3 layers are the most dominant participant in channel current. Interestingly, with a further increase in gate voltage, the polarization starts switching (from down to up) from the bottom layer of α-In_2Se_3 (Fig. S8b(iv)). At this point, the channel exhibits both up polarization (in first or first few bottom layers) and down polarization (in rest of the top layers) and that gives rise to a domain-wall (DW) within the channel. Note that, after the down to up polarization switching in bottom few α-In_2Se_3 layers, the minima of conduction band edge shifts from the bottom most layer to the vicinity of the DW. We refer such situation as the 'partially polarization switching' and in our considered case such phenomena happen at the gate voltage of ~30V. Now, with the decrease in gate voltage, the conduction band moves upward and consequently, current decreases rapidly. Such operation leads to clockwise hysteresis in I_D-V_{GS} characteristics.

- Low EOT devices:

Similar to the high EOT devices, with the increase in gate voltage channel current also increases in low EOT devices (as shown in Fig. S9b(i)-(iii)). Once the bottom layer polarization is switched at a certain positive gate voltage, further increase in gate voltage will induce a layer by layer gradual polarization switching. At the same time, the α-In_2Se_3 layer corresponding to the DW moves further from the bottom to the top α-In_2Se_3 layer. At a sufficiently high and positive gate voltage, all the layer will switch to polarization up and the corresponding band diagram is being depicted in Fig. S9b(iv)-(v). In such condition, both the top and bottom layers are conducting. Now, with the decrease in gate voltage, the conduction band edge near the bottom layers will start going above the fermi-level and therefore, the electron density contribution from bottom layer will decrease (Fig. S9b(v)-(vi)). However, the top layer is still conducting. Hence, a significant amount of current can be observed even at a negative gate voltage (-3.24V). However, at a sufficiently high negative voltage, all the α-In_2Se_3 layers will switch back to down polarization and consequently, the top layers will be no more conducting. Therefore, an abrupt decrease in current can be observed (as shown in Fig. S9b(vi)-(i)). Such operation leads to a counterclockwise hysteresis in I_{DS}-V_{GS} characteristics of FeS-FET.

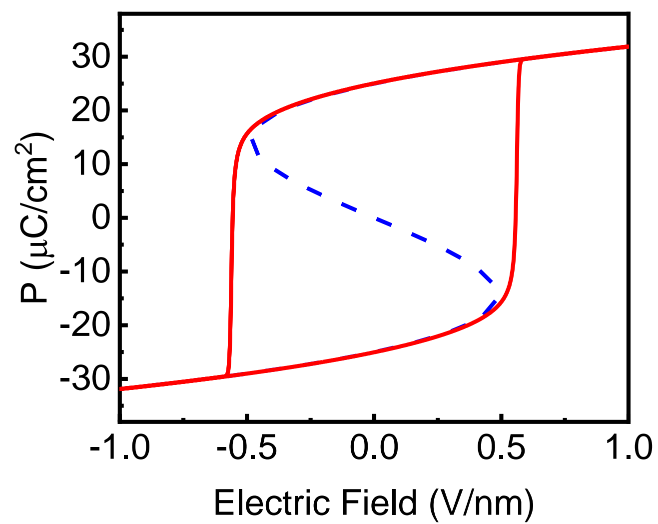

Figure S7. Polarization versus electric field characteristics by assumption in the simulation.

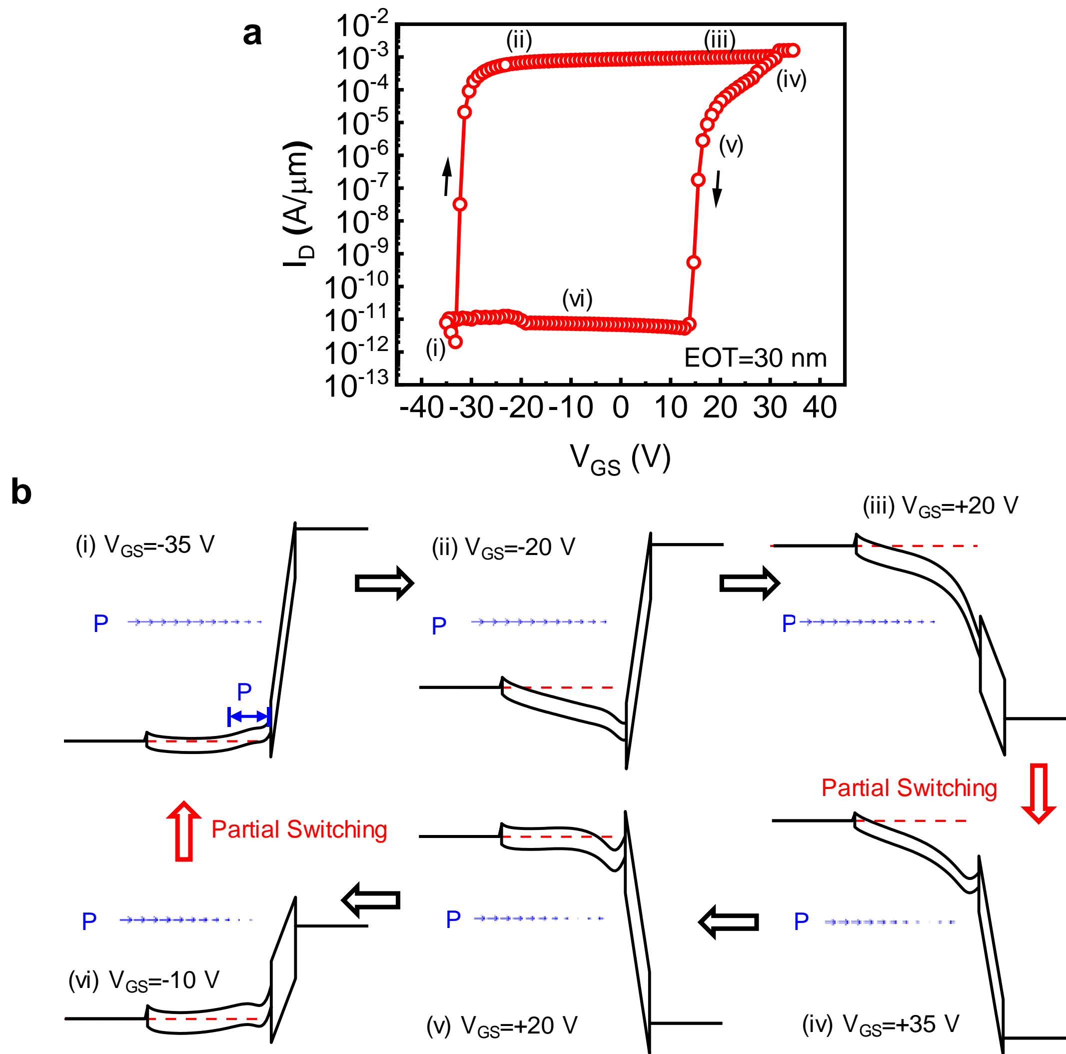

Figure S8. a, Simulation of I_D-V_{GS} characteristics of α-In_2Se_3 FeS-FET at EOT=30 nm. **b,** Band diagram and polarization vector map at different gate voltages during bi-directional gate voltage sweep. The direction of polarization vectors near insulator/semiconductor interface in (iv) and (v) is opposite to those in bulk and top surface.

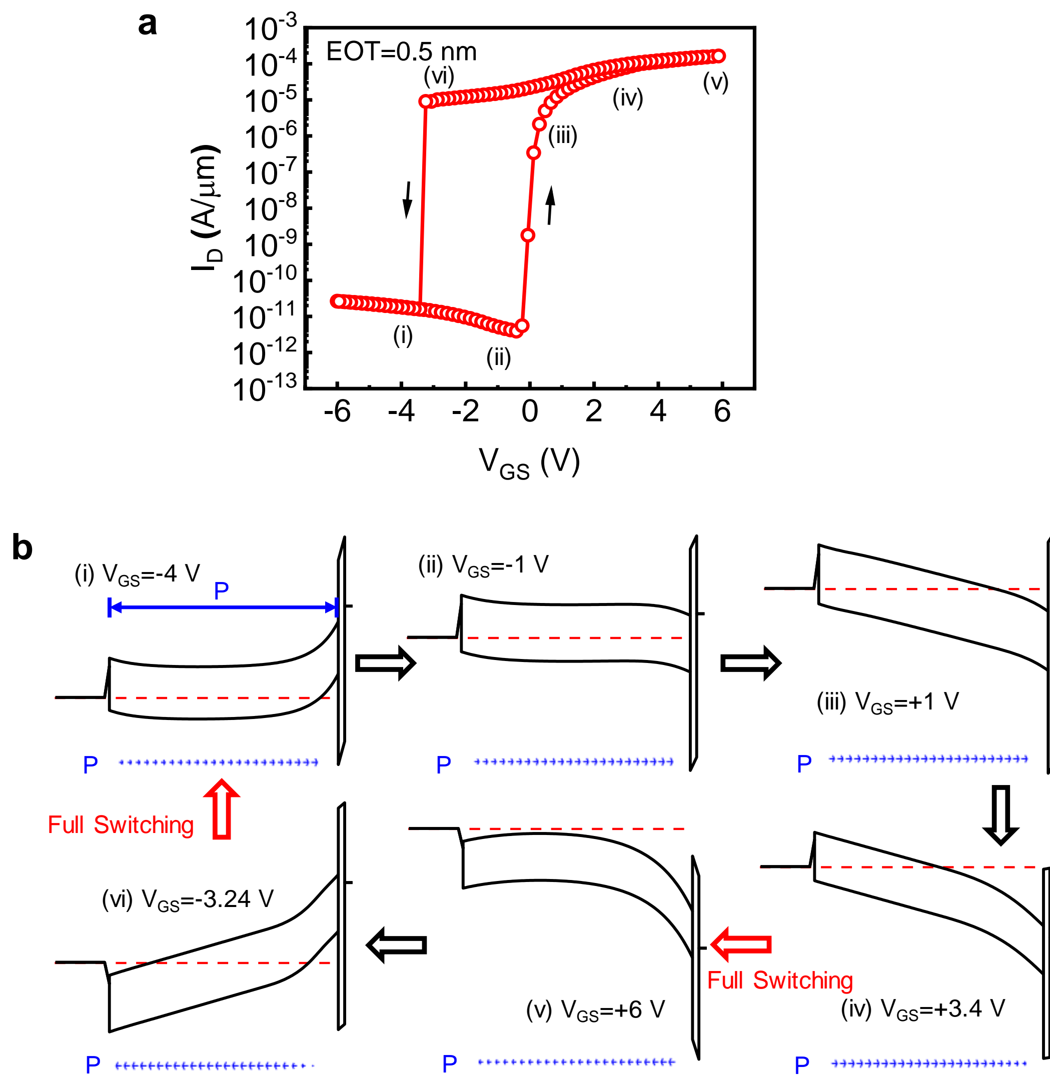

Figure S9. a, Simulation of I_D-V_{GS} characteristics of α-In_2Se_3 FeS-FET at EOT=0.5 nm. **b,** Band diagram and polarization vector map at different gate voltages during bi-directional gate voltage sweep.

7. Partial Switching of FeS-FET in Low EOT Condition

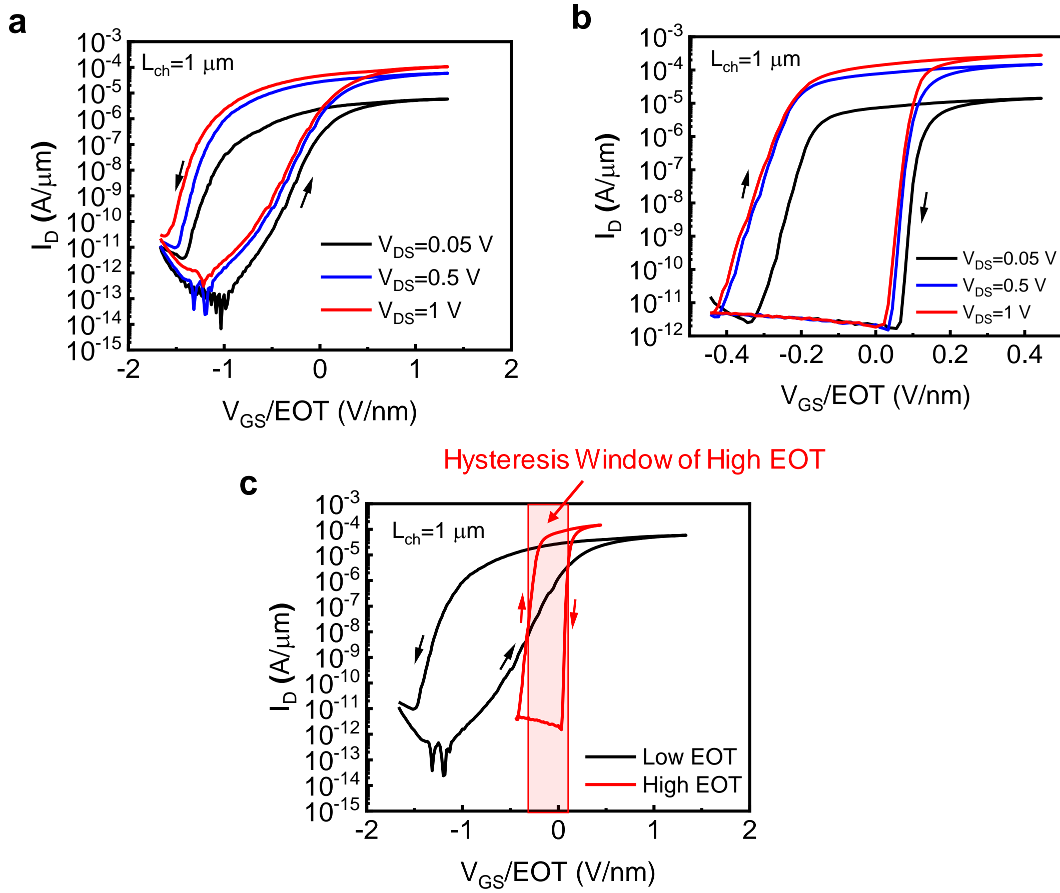

Figure S10. **a,** I_D as a function of V_{GS}/EOT for FeS-FET with low EOT. **b,** I_D as a function of V_{GS}/EOT for FeS-FET with high EOT. **c,** Comparison of I_D as a function of V_{GS}/EOT between low EOT and high EOT at V_{DS}=0.5 V.

To compare the electrical performance of α-In_2Se_3 FeS-FETs with different EOT under similar displacement field in gate oxide, we re-plot the transfer characteristics by introducing new x-axis as V_{GS}/EOT. Note that as displacement field is continuous (if no mobile charge), same displacement field in oxide is equivalent to same electric field in semiconductor. Fig. S10a shows I_D as a function of V_{GS}/EOT for a FeS-FET with low EOT and Fig. S10b shows I_D as a function of V_{GS}/EOT for a FeS-FET with high EOT. The slope in the subthreshold region is equal to SS/EOT by definition. Fig. S10c shows the comparison of I_D as a function of V_{GS}/EOT between low EOT and high EOT at V_{DS}=0.5 V. It is clear that device with high EOT shows a much sharper

slope (SS/EOT) in subthreshold region in this new I_D versus V_{GS}/EOT curve. SS/EOT is much smaller at high EOT condition. A direct result is that in the hysteresis window of high EOT condition (partial switching condition), as illustrated in Fig. S10c, the device with low EOT is either at off-state in the subthreshold region or at on-state. Therefore, if applying this partial switching condition to the device with low EOT, it cannot be effectively turn-on and turn-off. In addition, to change the electric field direction inside the semiconductor, on-state to off-state or off-state to on-state transitions are necessary (to change the direction of band bending). The change of applied electric field direction is the necessary condition of ferroelectric polarization switching in the ferroelectric semiconductor. In the on-state or off-state at low EOT condition, by applying same V_{GS}/EOT window, the electric field in the semiconductor doesn't even change the direction (Fig. S10(c)), so a partial switching induced clockwise hysteresis loop is difficult to achieve for low EOT devices.

8. A proposal of a deep steep-slope and hysteresis-free all ferroelectric Fe^2-FET

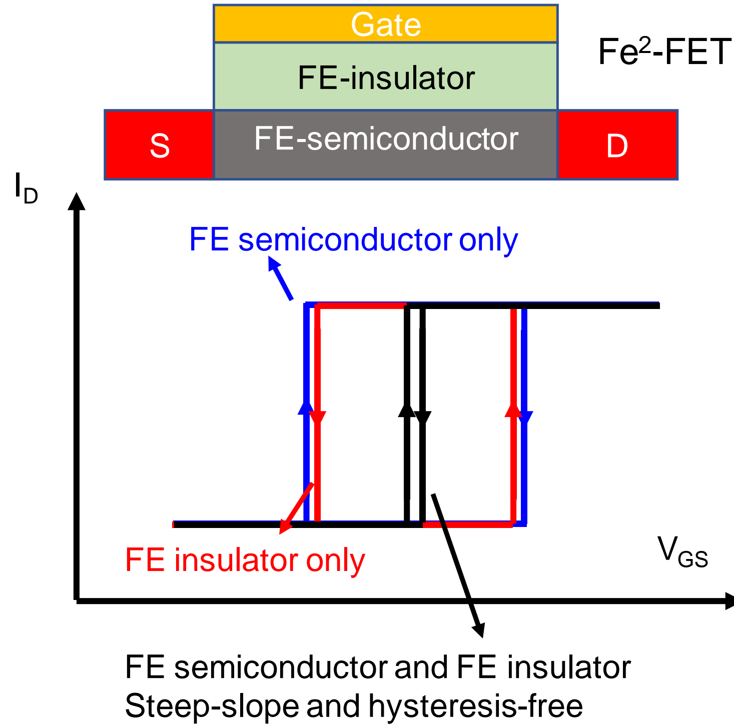

Figure S11. Illustration of a deep steep-slope and hysteresis-free ferroelectric insulator and ferroelectric semiconductor all ferroelectric field-effect transistors (Fe^2-FET).

As another step further by using the counterclockwise hysteresis of a Fe-FET and clockwise hysteresis of a FeS-FET, we propose to integrate a ferroelectric insulator on a ferroelectric semiconductor channel, as shown in Fig. S11 as a Fe^2-FET, to eliminate the hysteresis loops in both Fe-FET and FeS-FET and achieve a new type of deep steep-slope and hysteresis-free transistor. The key point is to match the two ferroelectric polarization charge so that the net ferroelectric polarization charge on the FE-insulator/FE-semiconductor interface is close to zero, so that hysteresis-free operation can be achieved.

References

1. Powell, M. J. Charge trapping instabilities in amorphous silicon-silicon nitride thin-film transistors. *Appl. Phys. Lett.* 43, 597–599 (1983).

2. Park, Y. *et al.* Thermally activated trap charges responsible for hysteresis in multilayer MoS_2 field-effect transistors. *Appl. Phys. Lett.* 108, 083102 (2016).

3. Schroder, D. K. *Semiconductor Material and Device Characterization*, (John Wiley & Sons, 2006).

4. L. Li *et al.* Quantum oscillations in a two-dimensional electron gas in black phosphorus thin films. *Nat. Nanotechnol.* 10, 608–613 (2015).